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A Novel Design of 32 Bit Unsigned Multiplier Using Modified CSLA

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Abstract - In VLSI design speed, power and chip area are the three conflicting constraints, most often considered in determining the performance and efficiency of the system. In this paper, the VLSI design of a high performance and low power 32-bit unsigned modified carry select adder (MCSLA) based multiplier using CBL term is been proposed and compared with the 32-bit unsigned conventional carry select adder (CSLA) based multiplier. Both the design of multiplier multiplies two 32-bit unsigned integer values and gives a product term of 64-bit value.The result analysis shows that the power area delay product reduction is possible with the proposed MCSLA based multiplier when compared to CSLA based multiplier. These two 32-bit unsigned multipliers are simulated using Modelsim and synthesized using Xilinx.

Index Terms- Area; CSLA; Delay; MCSLA; Power; Unsigned Multiplier; VHDL Modeling & Simulation.

1. INTRODUCTION

As the scale of integration is being growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip [3]. The Area speed of the system remains to be the two major design tools; power consumption has become a critical concern in today's VLSI system design [8]. As we know millions of instruction per second are performed in microprocessors. Hence, speed of operation is the most important constraint to be considered [3]. Due to device portability, miniaturization of device should be high and power consumption should be low. So, a VLSI designer has to optimize these three parameters in a design [2].

Addition usually impacts widely the overall performance of digital systems and is a crucial arithmetic function. In electronic applications, adders are most widely used as multipliers; Digital Signal Processor to execute various algorithms like Fast Fourier Transform (FFT), Finite Impulse Response (FIR) and Infinite Impulse Response (IIR).The Half-Adders (HA) are simplest single bit adders [1]. The full-adders are single bit adders with the provision of carry input (i/p) and output (o/p). The full-adders are typically composed of two Half-Adders (HA) hence are expensive than half-adders in terms of time, area and interconnection complexity [8]. The common approach for designing multi-bit adders is to form a chain of FA blocks by connecting the carry out bit of a FA to the carry in bit of the next FA block [1],[7][8].

Multiplication is one of the basic arithmetic operations. Multiplication operation is also called as a adding and shifting method [5], [8]. Multiplication operation involves two methods: one is Generation of partial products and another one is summation. The speed of multiplication mainly depends on the Partial product generation and/or summation. Therefore, using high speed multipliers is a critical requirement for high performance processors [5], [6], [7].

Our study is focused on the comparative analysis of adders implemented as a multipliers based on area, power consumption and time needed for calculation. In this paper, the VLSI design of 32-bit unsigned modified carry select adder (MCSLA) based multiplier using CBL term is been proposed and compared with the 32-bit unsigned conventional carry select adder (CSLA) based multiplier. Here the two unsigned 32-bit multipliers multiplies (N*N) and gives the product term as 64-bit (2N) output [1], [8]. To model and simulate the multiplier design a VHDL, Very high speed integrated circuit Hardware Description Language was used [2], [3].

Hence design of area and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. Our main interest must be on design of a better architecture of basic building block i.e. adder [1]. So, we need Digital Signal Processing (DSP) style system for area efficient, less delay and low power consumption [6]. Our basic building block must dominate in Digital Signal Processing (DSP) application, VLSI architecture and where ever reduced delay is needed is needed.

2. CARRY SELECT ADDER

A conventional carry select adder (CSLA) is an RCA–RCA configuration which has two units: SCG (The sum and carry generator unit) and SCS (The sum and carry selection unit) [1], [4] and [8].In Sum Carry Generation unit (SCG), a pair of sum bits and output-carry bits corresponding to the anticipated input-carry (C_{in} =0 and C_{in}=1) are generated [7]. In Sum Carry

Selection unit (SCS) we compute these alternative results in parallel and subsequently selecting one out of each pair for final-sum and final-output-carry with single or multiple stages of hierarchical techniques. The correct computation is chosen when C_{in} is delivered, with the help of a multiplexer to get the desired output [7], [4]. The structure of conventional CSLA is shown in Fig. 1.

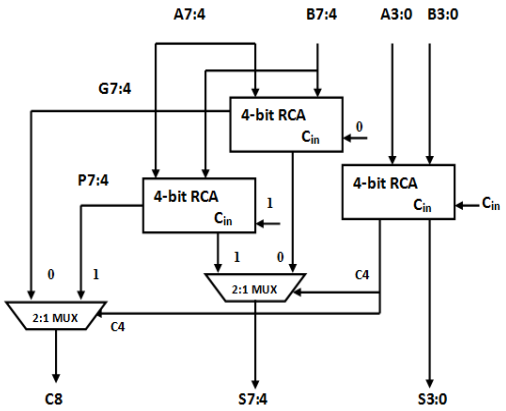

Fig.1. Conventional carry select adder

In general, we can write the algorithm as:
If Carry in =1, then the sum and carry out are given by,

Sum (i) =a (i) xor b (i) xor '1' (1)

Carry (i+1) = (a (i) and b (i)) or (b (i) or a (i)) (2)

If Carry in =0, then the sum and carry out are given by,

Sum (i) = a (i) xor b (i) (3)

Carry (i+1) = a (i) and b (i) (4)

The sum function:

$$S_i = C_i S_i^0 + C_i S_i^1 \quad (5)$$

The carry function:

$$C_{i+1} = C_i C_{i+1}^0 + C_i C_{i+1}^1 \quad (6)$$

The carry select adder is used in many digital computational systems to reduce the problem of propagation delay [7], [9]. The speed is improved with this technique by saving the time used for computation [4]. The conventional carry select adder (CSLA) is not efficient in the case of area because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input C_{in} =0 and C_{in} =1 separately. The SCG unit consumes most of the logic resources of CSLA and significantly contributes to the critical path [4], [8].

3. PROPOSED MODIFIED CSLA USING COMMON BOOLEAN LOGIC

To remove the duplicate adder cells in the conventional CSLA, an area efficient CSLA is proposed by sharing Common Boolean Logic (CBL) term in Sum Carry Generation unit [9]. The main idea of this work is to use CBL term instead of RCA with carry C_{in} =1, in order to reduce the area and power of conventional CSLA. Thus, modified CSLA (MCSLA) is designed such that it occupies less area and has low power consumption than conventional CSLA. The structure of Proposed MCSLA is shown in Fig. 2.

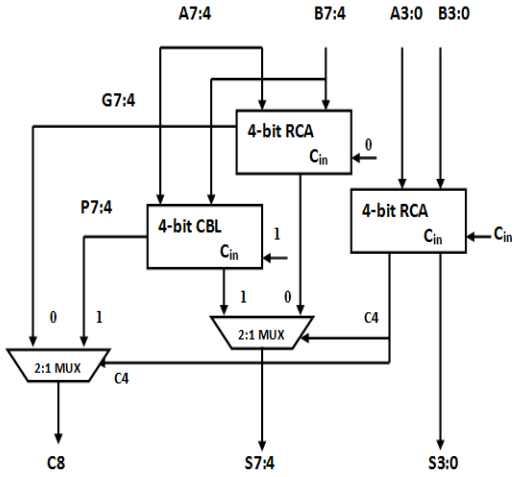

Fig.2. Proposed modified carry select adder using CBL term.

To share the Common Boolean Logic term, we only need to implement an XOR gate and one INV gate to generate the summation pair. And to generate the carry pair, we need to implement one OR gate and one AND gate. In this way, the summation and carry circuits can be kept parallel.

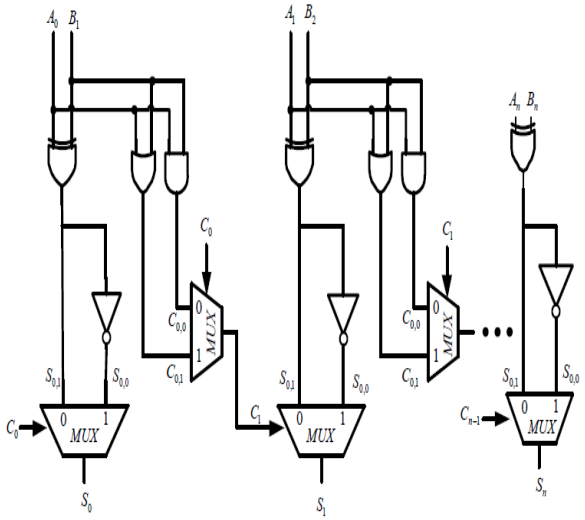

Fig.3. Internal structure of the proposed modified carry select adder constructed by sharing the common boolean logic term.

In general, we can write the algorithm as:
If Carry in =1, then the sum and carry out are given by,

Sum (i) =a (i) xor b (i). (7)

Carry (i+1) = a (i) or b (i) (8)

If Carry in =0, then the sum and carry out are given by,

Sum (i) = (a (i) xor b (i))' (9)

Carry (i+1) = a (i) and b (i) (10)

The sum function:

$S_i = C_i S_i^0 + C_i S_i^1$ (11)

The carry function:

$C_{i+1} = C_i C_{i+1}^0 + C_i C_{i+1}^1$ (12)

TABLE I: Truth Table of single bit full adder, where the upper half part is the case of C_{in}=0 and the lower half part is the case of C_{in}=1

C_{in}	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

While analyzing the truth table of single bit full adder, result shows that the output of summation signal as carry-in signal is logic "0" is inverse signal of itself as carry-in signal is logic "1" [1].The speed is improved with this technique by saving the time used for computation. The area occupied and power required for this design is less when compared to conventional CSLA because CBL term is used instead of an RCA for C_{in} =1, to generate partial sum and carry [1].

4. UNSIGNED MULTIPLIER

The multiplier is one of the hardware key blocks in Digital signal processing techniques [6]. The multiplier involves generation of partial products, one for each digit in the multiplier as in Fig.4.These partial products are then summed to produce the final product. The N-bit multiplier multiplies two N-bit values and gives the final product term as a 2N-bit value [2], [8], [9]. A Partial Schematic of 32-bit Unsigned Multiplier is shown in Fig.4.

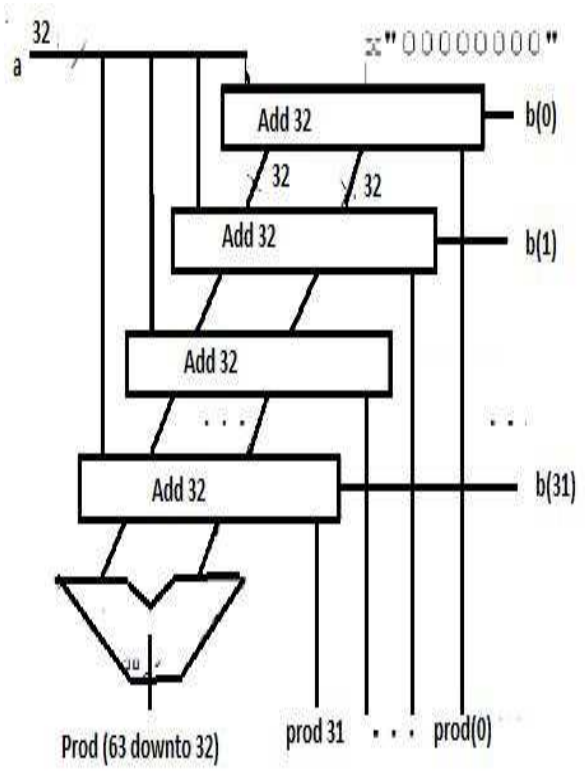

Fig.4. A partial schematic of unsigned multiplier

We use the following algorithm to implement the multiplication operation for unsigned data [10].

5. MULTIPLICATION ALGORITHM

Let the product register size be 64 bits and the multiplicand register size is 32 bits. Store the multiplier in the least significant half of the product register. Clear the most significant half of the product register [2], [8], [10].

Repeat the following steps for 32 times:

1. If the least significant bit (LSB) of the product register is "1" then add the multiplicand to the most significant (MSB) half of the product register.
2. Shift the content of the product register one bit to the right (ignore the shifted-out bit).
3. Shift-in the carry bit into the most significant bit of the product register.

The flow chart for the multiplication algorithm is shown in Fig.5.

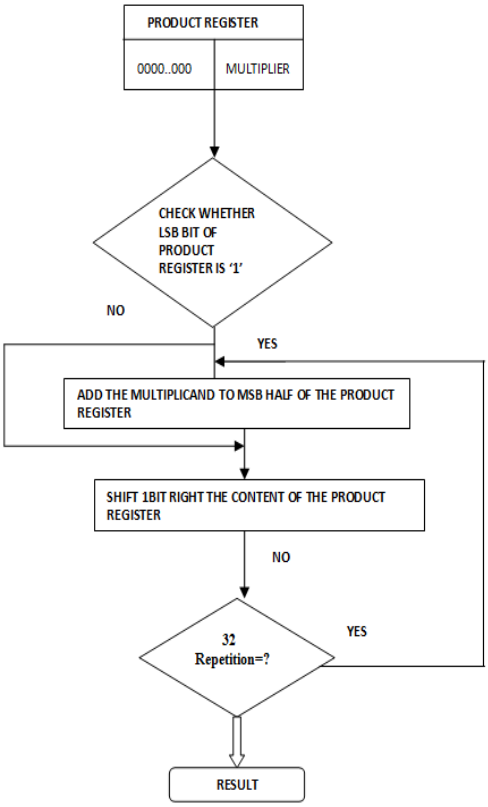

Fig.5. Flow chart of multiplication algorithm

The block diagram for n-bit Multiplier using the multiplication algorithm [8], [9], [10] is shown in Fig.6.

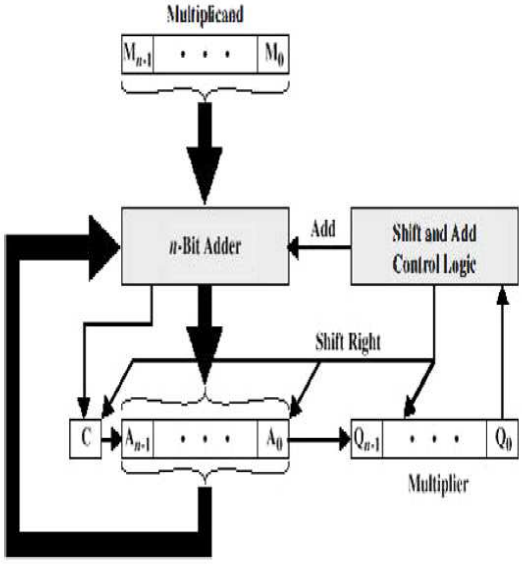

Fig.6. Multiplier block diagram for two n-bit values

6. VHDL SIMULATION RESULTS

The VHDL model for both the 32-bit unsigned multipliers has been simulated using Modelsim and synthesized using Xilinx and presented in this section [9], [10].

6.1. *32-bit unsigned CSLA multiplier*

6.1.1. *Schematic*

Fig.7. Schematic of 32-bit unsigned CSLA multiplier

6.1.2. *Simulation result*

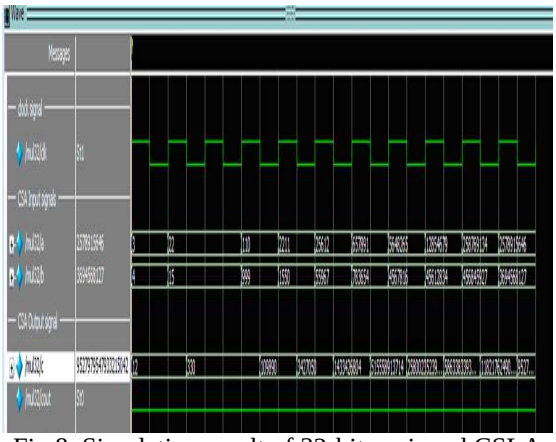

Fig.8. Simulation result of 32-bit unsigned CSLA multiplier

6.2. *32-bit unsigned MCSLA multiplier*

6.2.1. *Schematic*

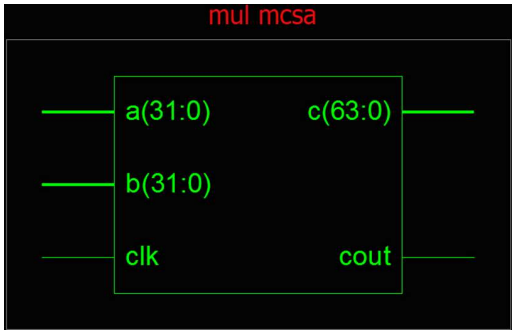

Fig.12. Schematic of 32-bit unsigned MCSLA multiplier

6.2.2. *Simulation result*

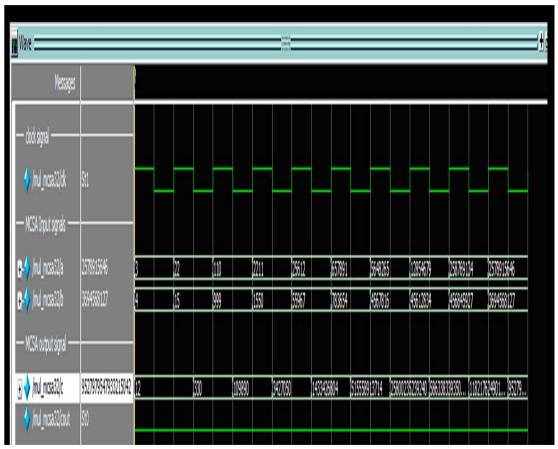

Fig.13. Simulation result of 32-bit unsigned MCSLA multiplier

TABLE II: Performance comparison of proposed MCSLA with CSLA

Multiplier Type	Delay (ns)	Area	Power (W)	Delay Area Power Product
CSLA Based Multiplier	126.9	3677 logic cells	0.081	37795.5
MCSLA Based Multiplier	105.8	2045 logic cells	0.079	17092.5

The performance comparison of 32-bit unsigned proposed modified carry select adder (MCSLA) based multiplier with the 32-bit unsigned conventional carry select adder (CSLA) based multiplier is shown in Table. II.

7. CONCLUSION

In VLSI design Power, delay and area are the most important factors that limits the performance of any circuit. This work presents a simple approach to reduce the area, delay and power used to design CSLA architecture. The regular carry select adder has the disadvantage of more power consumption, more delay and occupying more chip area. In this paper, the VLSI design of a high performance and low power 32-bit unsigned proposed modified carry select adder (MCSLA) based multiplier using CBL term is been proposed and compared with the 32-bit unsigned conventional carry select adder (CSLA) based multiplier. The result analysis shows that the **45%** power area delay product reduction is possible with the use of the proposed MCSLA based multiplier compared to conventional CSLA based multiplier.

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